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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/669,539	09/24/2003	Robert-Christian Hagen	MAS-FIN-406	4640

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LERNER AND GREENBERG, PA
P O BOX 2480
HOLLYWOOD, FL 33022-2480

EXAMINER	
HA, NATHAN W	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 03/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/669,539	HAGEN ET AL.	
	Examiner	Art Unit	
	Nathan W. Ha	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) *1-12* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group II, claim 13-21, in the reply filed on 12/9/04 is acknowledged.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 13-14, 16-17, and 20-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Saeki (US 6,717,252).

In regard to claim 13, in fig. 2, Saeki discloses a rewiring substrate 30 having a central area with connecting pads 32 for forming flip chip connections, having edge areas with connecting pads, also, 32;

at least one first lower electronic module formed by a semiconductor chip, first chip, 10A, said lower electronic module having contact areas electrically connected using flip chip technology to said connecting pads in said central area of the rewiring

substrate, the lower electronic module having a passive rear face, or inactive surface face;

at least one second upper electronic module 20, second chip, including a rewiring structure (the rewiring structure connected to wires 43, for example) and a semiconductor chip with external contact surfaces, said upper electronic module having a passive rear face, or inactive surface) resting against said passive rear face of the lower electronic module;

a plurality of bonding connections 22 and 23 between the external contact surfaces of the upper electronic module and the connecting pads in said edge areas and the rewiring substrate; and

a component package 44 surrounding the lower electronic module and said lower electronic module.

In regard to claim 14, Saeki further discloses

a protective sheath 16, for example;

the component package having material, resin, for example; and

the protective sheath forming a material boundary with the material of said component package.

In regard to claim 16, Saeki further discloses, wherein:

the rewiring substrate includes a printed circuit board 30 (as mentioned above) having an upper face with structured metal layers, for example pads 32, a lower

face with structured metal layers, pads 33, for example, and through-contacts, or via, 34 electrically connecting said structured metal layers on the upper face and the lower face;

the lower face of said printed circuit board has external contact surfaces, bottom surface, for example with external contacts 35;

the upper face of said printed circuit board has the central area with said connecting pads (mentioned above) for forming flip chip connections;

the upper face areas with the printed circuit board has the edge connecting pads, also, 32 in the edge areas of the rewiring substrate; and

the upper face of the printed circuit board has rewiring substrate lines between the connecting pads for forming flip chip connections and the through-contacts (see fig. 2).

In regard to claim 17, Saeki further discloses an adhesive layer 42 configured between the passive rear face of the upper electronic module and the passive rear face of the lower electronic module (see also, fig.2).

In regard to claim 20, Saeki further discloses, wherein:

the connecting pads of the rewiring substrate have surfaces and surfaces of said connecting pads of the rewiring substrate point in a first direction;

the external contact surfaces of the rewiring structure have surfaces and the surfaces of said external contact surfaces of the rewiring structure point in the first direction (see fig. 2).

In regard to claim 21, wherein the plurality of bonding connections include a bonding wire 43 forming a bonding clip running from one of the connecting pads on said rewiring substrate to a corresponding one of the external contact surfaces on said upper electronic module (see fig. 2).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Saeki as applied to claims 13-14 above, and further in view of Butler (US 6,392,304).

In regard to claim 15, Saeki discloses all of the claimed limitations as mentioned above. Saeki further discloses that the second chip is stacked over the first chip. Saeki, however, does not expressly teach that the chips are logic and memory chips. It should be noted that semiconductor chips are composed of IC circuits in general. In some cases they can be interchangeable. For instance, Butler discloses a package including a stack chip structure where one chip is a logic chip and the other is memory chip in order to reduce the levels of capacitance and inductance and increase the speeds at reduced levels of power consumption, see the abstract.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to easily recognize a feature of stacking two different

chips on a substrate in order to reduce the levels of capacitance and inductance and increase the speeds at reduced levels of power consumption.

6. Claims 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saeki as applied to claims 13-14 above, and further in view of Khiang et al. (US 2003/0197284, hereinafter, Khiang.)

In regard to claims 18 and 19, Saeki discloses all of the claimed limitations as mentioned above except the upper chip has an active upper surface configured with a central bonding channel that has bonding connections and the sheath for bonding channel and the connections.

Khiang, in fig. 4a, discloses an analogous package comprising a substrate 63, first chip 61, a second chip 73 stacked over the first chip, and the second chip further comprises a central connection portion 74 and a sheath 76 for bonding connections in order to facilitate the attachment of electrical connections and reduce the risk of interference of the electrical connections (see section [0030].)

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to introduce more electrical connections at the central of the chip in order to facilitate the attachment of electrical connections and reduce the risk of interference of the electrical connections.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nathan W. Ha whose telephone number is (571) 272-1707. The examiner can normally be reached on M-TH 8:00-7:00(EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nathan Ha
March 16, 2005